

Figure 1

Memory Bus Peripheral (FPGA) Operation

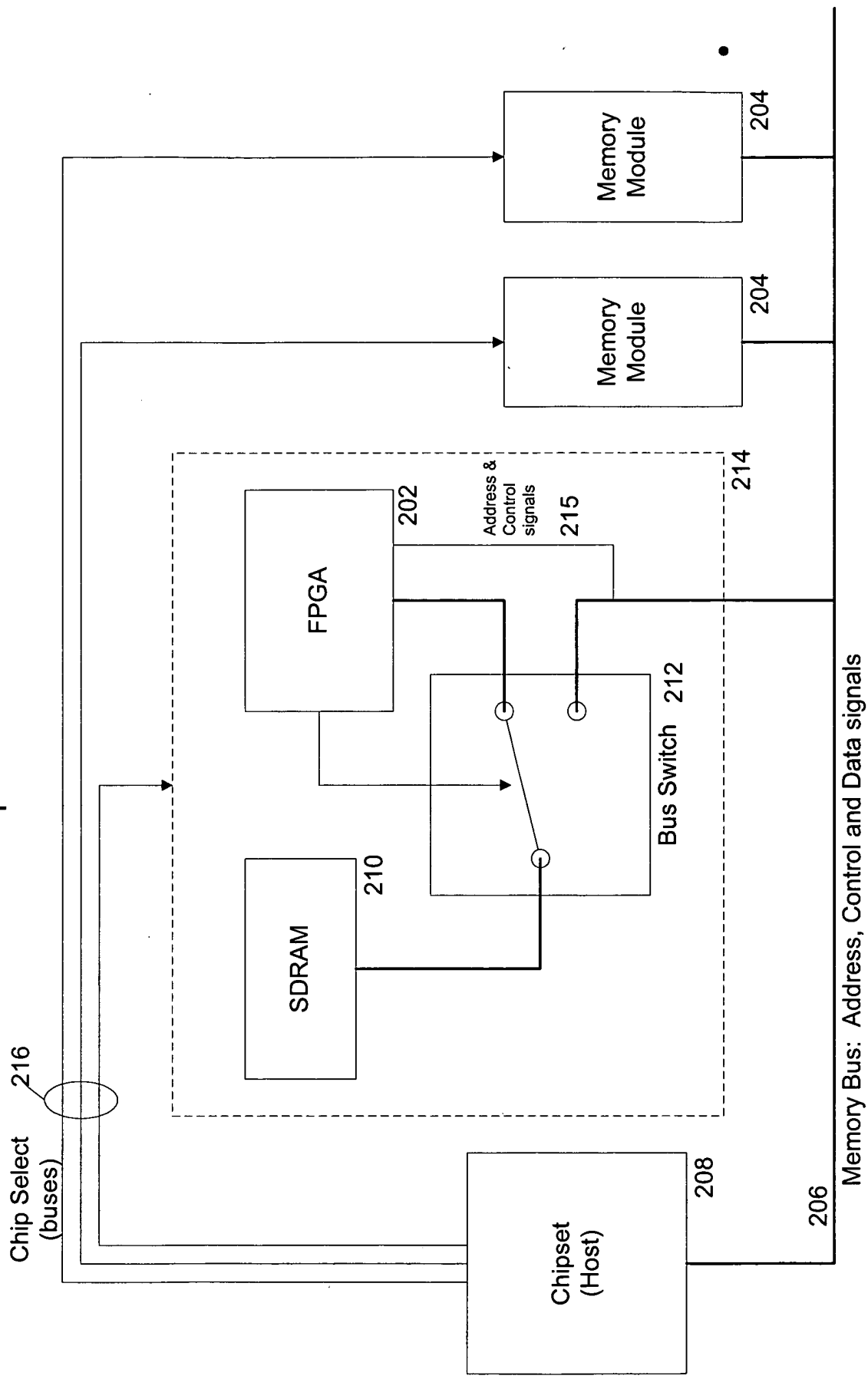


Figure 2

Operational Flowchart

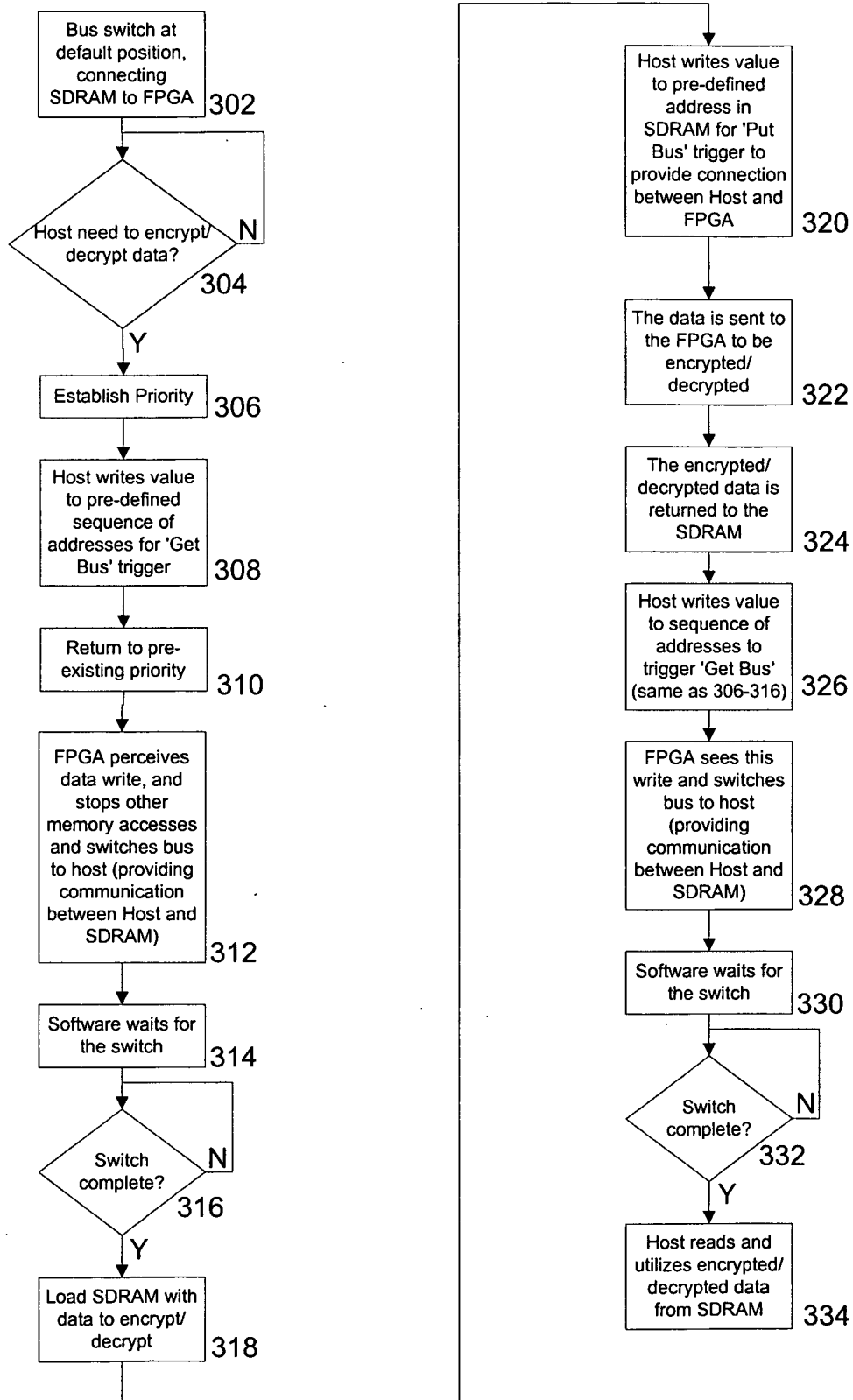


Figure 3

Example Memory Module Trigger Address Locations

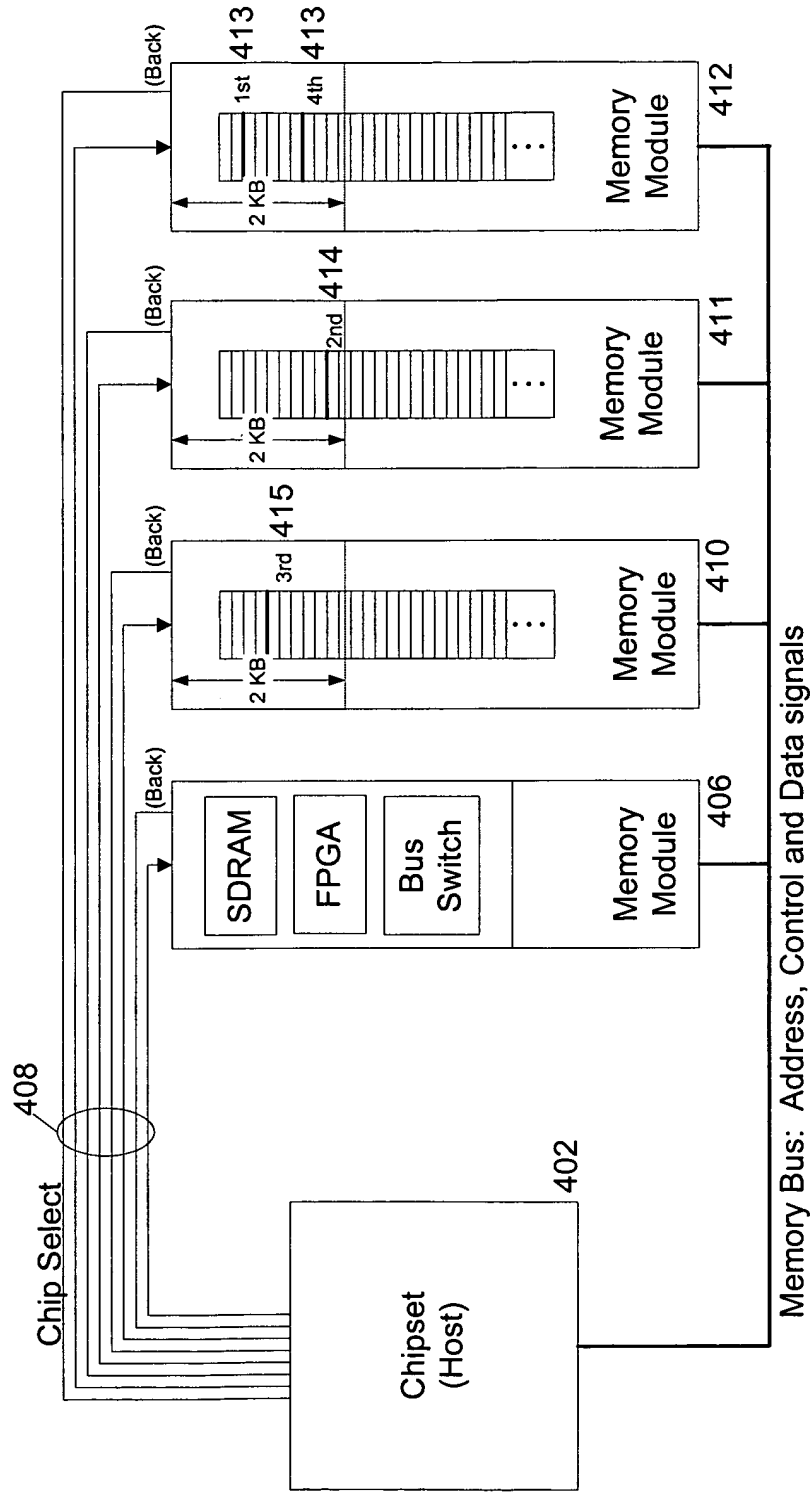


Figure 4